

Appl. No. 10/050,246
Amdt dated Jan 15, 2004
Reply to Office Action of Nov 18, 2003

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (previously presented) A barrier stack comprising:
 - a first barrier layer having a top surface; and
 - a thin intermediate layer on the top surface of the first barrier layer formed by a thermal process in an oxidizing ambient, the thin intermediate layer providing elements to stuff the grain boundaries on or near the top surface of the first barrier layer;
 - a second barrier layer on the thin intermediate layer, wherein the grain boundaries of the first and second barrier layer are mismatched, the stuffed grain boundaries of the first barrier layer and mismatched grain boundaries of the first and second barrier layers enhance the barrier properties of the barrier stack.
2. (previously presented) The barrier stack of claim 1 wherein the barrier layer serves as a barrier layer for a capacitor over plug structure having:
 - a capacitor having a capacitor dielectric layer disposed between first and second electrodes; and
 - a plug electrically coupled to the first electrode wherein the barrier stack is disposed between the plug and first electrode to reduce oxidation of the plug.
3. (previously presented) The barrier stack of claim 2 wherein the capacitor over plug structure further comprises an adhesion layer between the barrier stack and the plug.
4. (previously presented) The barrier stack of claim 2 wherein the capacitor of the capacitor over plug structure comprises a ferroelectric capacitor having a ferroelectric layer disposed between first and second electrodes.
5. (original) The barrier stack of claim 4 further comprises an adhesion layer between the barrier stack and plug.

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6. (previously presented) The barrier stack of claim 1, 2, 3, 4, or 5 wherein the oxidizing ambient comprises oxygen, ozone or NO_{x(0<x<2)} to form the intermediate layer comprising an oxide, the oxidizing ambient providing elements comprising oxygen.
7. (previously presented) The barrier stack of claim 6 further comprises a second thin intermediate layer on a top surface of the second barrier layer formed by thermal process in oxidizing ambient, the second thin intermediate layer providing elements to stuff the grain boundaries on or near the top surface of the second barrier layer.
8. (previously presented) The barrier stack of claim 7 wherein the thermal process comprises rapid thermal oxidation.
9. (cancelled)
10. (cancelled)
11. (cancelled)
12. (cancelled)
13. (previously presented) The barrier stack of claim 6 wherein the thermal process comprises rapid thermal oxidation.
14. (cancelled)
15. (previously presented) The barrier stack of claim 6 wherein the barrier layers comprise a material selected from the group of materials comprising Ir, Rh, Ru, Pd, or alloys thereof, wherein the first and second barriers are formed from same or different materials.
16. (cancelled)

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17. (cancelled)

18. (cancelled)

19. (previously presented) The barrier stack of claim 13 wherein the barrier layers comprise a material selected from the group of materials comprising Ir, Rh, Ru, Pd, or alloys thereof, wherein the first and second barriers are formed from same or different materials.

20. (cancelled)

21. (cancelled)

22. (cancelled)

23. (previously presented) The barrier stack of claim 7 wherein the barrier layers comprise a material selected from the group of materials comprising Ir, Rh, Ru, Pd, or alloys thereof, wherein the first and second barriers are formed from same or different materials.

24. (previously presented) The barrier stack of claim 8 wherein the barrier layers comprise a material selected from the group of materials comprising Ir, Rh, Ru, Pd, or alloys thereof, wherein the first and second barriers are formed from same or different materials.

25. (cancelled)

26. (cancelled)

27. (previously presented) A capacitor over plug structure comprising:
a capacitor having first and second electrodes separated by a capacitor dielectric layer;
a plug coupling the first electrode of the capacitor; and
a barrier stack disposed between the plug and the first electrode comprising:
a first barrier layer having a top surface;

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a intermediate layer on the top surface of the first barrier layer formed by a thermal process in an oxidizing ambient, the thin intermediate layer providing elements to stuff the grain boundaries on or near the top surface of the first barrier layer; and

a second barrier layer on the thin intermediate layer, wherein the grain boundaries of the first and second barrier layer are mismatched, the stuffed grain boundaries of the first barrier layer and mismatched grain boundaries of the first and second barrier layers enhance the barrier properties of the barrier stack to reduce oxidation of the plug.

28. (previously presented) The capacitor over plug structure of claim 27 wherein the capacitor comprises a ferroelectric capacitor.

29. (previously presented) The capacitor over plug structure of claim 27 or 28 wherein the oxidizing ambient comprises oxygen, ozone or $\text{NO}_{x(0 < x < 2)}$, the thermal process forms the intermediate layer comprising an oxide and the oxidizing ambient provides elements comprising oxygen to stuff the grain boundaries.

30. (previously presented) The capacitor over plug structure of claim 29 wherein the thermal process comprises rapid thermal oxidation.

31. (previously presented) The capacitor over plug structure of claim 30 wherein the barrier layers comprise a material selected from the group of materials comprising Ir, Rh, Ru, Pd, or alloys thereof, the barrier layers can be formed from same or different materials.

32. (previously presented) The capacitor over plug structure of claim 29 further comprises a second intermediate layer on a top surface of the second barrier layer formed by thermal process in oxidizing ambient, the second intermediate layer providing elements to stuff the grain boundaries at or near the top surface of the second barrier layer.

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33. (previously presented) The capacitor over plug structure of claim 32 wherein the barrier layers comprise a material selected from the group of materials comprising Ir, Rh, Ru, Pd, or alloys thereof, the barrier layers can be formed from same or different materials.
34. (previously presented) The capacitor over plug structure of claim 33 wherein the thermal process comprises rapid thermal oxidation.
35. (currently amended) The capacitor over plug structure of claim [34] 27 wherein the barrier layers comprise a material selected from the group of materials comprising Ir, Rh, Ru, Pd, or alloys thereof, the barrier layers can be formed from same or different materials.
36. (previously presented) The capacitor over plug structure of claim 29 wherein the barrier layers comprise a material selected from the group of materials comprising Ir, Rh, Ru, Pd, or alloys thereof, the barrier layers can be formed from same or different materials.
37. (withdrawn) A method of forming a capacitor over plug structure comprising:
providing a substrate having an interlevel dielectric layer formed thereon and a plug formed in the interlevel dielectric layer; and
forming a barrier stack on the dielectric layer comprising:
forming a first barrier layer on the interlevel dielectric layer in contact with a top surface of the plug;
annealing the first barrier layer in oxidizing ambient to form an intermediate layer on a top surface of the first barrier layer and to stuff grain boundaries at or near a top surface of the first barrier layer with elements;
forming a second barrier layer above the intermediate layer wherein grain boundaries of the first and second barrier layers are mismatched; and
forming a capacitor over the barrier stack, the capacitor comprises first and second electrodes separated by a capacitor dielectric layer, wherein the barrier stack reduces oxidation of the plug.

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38. (withdrawn) The method of claim 37 wherein annealing in the oxidizing ambient comprises annealing in oxygen, ozone or $\text{NO}_{x(0 < x < 2)}$ to provide elements comprising oxygen.
39. (withdrawn) The method of claim 38 wherein annealing comprises rapid thermal oxidation.
40. (withdrawn) The method of claim 39 wherein forming the first and second barrier layers comprises depositing materials comprising Ir, Rh, Ru, Pd, or alloys thereof to form the barrier layers, wherein forming the first and second barrier layers need not deposit the same material.
41. (withdrawn) The method of claim 38 further comprises forming annealing the second barrier layer in oxidizing ambient to form a second intermediate layer on a top surface of the second barrier layer and to stuff grain boundaries at or near a top surface of the second barrier layer with elements.
42. (withdrawn) The method of claim 41 wherein forming the first and second barrier layers comprises depositing materials comprising Ir, Rh, Ru, Pd, or alloys thereof to form the barrier layers, wherein forming the first and second barrier layers need not deposit the same material.
43. (withdrawn) The method of claim 41 wherein annealing comprises rapid thermal oxidation.
44. (withdrawn) The method of claim 38 wherein forming the first and second barrier layers comprises depositing materials comprising Ir, Rh, Ru, Pd, or alloys thereof to form the barrier layers, wherein forming the first and second barrier layers need not deposit the same material.

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45. (withdrawn) The method of claim 39 wherein forming the first and second barrier layers comprises depositing materials comprising Ir, Rh, Ru, Pd, or alloys thereof to form the barrier layers, wherein forming the first and second barrier layers need not deposit the same material.
46. (withdrawn) A method of forming a barrier stack comprising:
providing a substrate prepared with a device layer;
forming a first barrier layer on the device layer;
annealing the first barrier layer in oxidizing ambient to form an intermediate layer over a top surface of the first barrier layer and to stuff grain boundaries at or near a top surface of the first barrier layer with elements; and
forming a second barrier layer above the intermediate layer, wherein grain boundaries of the first and second barrier layers are mismatched.
47. (withdrawn) The method of claim 46 wherein the device layer comprises a interlevel dielectric layer with a plug formed therein and the barrier stack is in contact with the plug.
48. (withdrawn) The method of claim 46 wherein the device layer comprises a interlevel dielectric layer with a plug formed therein and the barrier stack is in contact with the plug and further comprises forming a ferroelectric capacitor having first and second electrodes separated by a ferroelectric layer over the barrier stack.
49. (withdrawn) The method of claim 46, 47 or 48 wherein annealing in the oxidizing ambient comprises annealing in oxygen, ozone or $\text{NO}_{x(0 < x < 2)}$ to provide elements comprising oxygen.
50. (withdrawn) The method of claim 49 wherein annealing comprises rapid thermal oxidation.

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51. (withdrawn) The method of claim 50 wherein forming the first and second barrier layers comprises depositing materials comprising Ir, Rh, Ru, Pd, or alloys thereof to form the barrier layers, wherein forming the first and second barrier layers need not deposit the same material.
52. (withdrawn) The method of claim 49 further comprises forming annealing the second barrier layer in oxidizing ambient to form a second intermediate layer on a top surface of the second barrier layer and to stuff grain boundaries at or near a top surface of the second barrier layer with elements.
53. (withdrawn) The method of claim 52 wherein forming the first and second barrier layers comprises depositing materials comprising Ir, Rh, Ru, Pd, or alloys thereof to form the barrier layers, wherein forming the first and second barrier layers need not deposit the same material.
54. (withdrawn) The method of claim 52 wherein annealing comprises rapid thermal oxidation.
55. (withdrawn) The method of claim 54 wherein forming the first and second barrier layers comprises depositing materials comprising Ir, Rh, Ru, Pd, or alloys thereof to form the barrier layers, wherein forming the first and second barrier layers need not deposit the same material.
56. (withdrawn) The method of claim 49 wherein forming the first and second barrier layers comprises depositing materials comprising Ir, Rh, Ru, Pd, or alloys thereof to form the barrier layers, wherein forming the first and second barrier layers need not deposit the same material.